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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,377	LIPPINCOTT ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-29 are pending.

Claim Objections

2. Objection is withdrawn in light of Applicant's amendments.

Claim Rejections - 35 USC § 112

3. Rejection is withdrawn in light of Applicant's amendments.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-9 and 11-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt (U.S. Patent No. 5,410,723) in view of Okamoto (U.S. Patent No. 5,729,711)

2. Regarding claim 1, Schmidt discloses a data driven processing method (col 1 lines 13-15), comprising: providing a first set of instructions and incoming data to a first processing unit (fig. 7; col 9 lines 26-49), of a data driven processor (col 1 lines 13-15),

to operate upon said incoming data; configuring a data path for transferring data between a second processing unit of the data driven processors (col. 4 lines 37-40); and the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path (col 2 lines 20-26).

The disclosed data memory suggests the use of load/store instructions which satisfy the remaining limitations of the claim.

Schmidt fails to disclose that the processing units are interconnected to an external memory.

Okamoto discloses the use of an external memory accessible by each of the data driven processors (figs. 5, 6, and 7).

Schmidt would have been motivated to utilize the external memory in order to allow coherency of memory operations and a simplistic method of exchanging information. This is particularly true when Schmidt desires to have the processing units of the array exchange information (col 3 lines 5-7) and they can be arranged into a rectangular or even one-dimensional structure that would allow each processing element to gain easy memory access (col 3 lines 51-55).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing unit of Schmidt and allow it to access an external memory as in Okamoto.

3. Regarding claim 2, Schmidt/Okamoto discloses the method of claim 1 wherein the processing unit recognizes an image processing motion vector in said first set of instructions, and said additional data is to be written to the external memory and includes a macro block generated by the second processing unit based on the motion vector (col 4 lines 37-60)

4. Regarding claim 3, Schmidt/Okamoto discloses the method of claim 1 wherein the data path is configured by an external host controller (Okamoto Fig. 5 I/O unit).

5. Regarding claim 4, Schmidt/Okamoto discloses the method of claim 1 further comprising: the first processing unit providing an indication to the memory access unit of whether transfer is one of a read or write (Okamoto col 2 lines 30-45)

6. Regarding claim 5 Schmidt/Okamoto discloses a data processor (col 1 lines 13-15) comprising: a first direct memory access (DMA) unit (fig. 3); and a plurality of processing units (col 3 lines 51-55) each having a plurality of data ports (fig. 1a), the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the DMA unit (fig. 1a; col 3 lines 5-7; Okamoto figs. 5, 6, 7 as combined), the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port

wherein the input port is programmable to route incoming data to any one of the output ports (col 3 lines 5-7), wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and a result data by one of the processing units is transferred (Okamoto Figs. 5, 6, and 7).

7. Regarding claim 6, Schmidt/Okamoto discloses the processor of claim 5 further comprising: memory interface circuitry, wherein the DMAN unit is to access external memory via the memory interface circuitry (Okamoto Figs. 5, 6, and 7).

8. Regarding claim 7, Schmidt/Okamoto discloses the processor of claim 6 further comprising a host interface through which a host processor is to configure data flow between the data ports, wherein the memory interface circuitry is on-chip with the DMA unit, the plurality of processing units, and the host interface (col 3 lines 50-55).

9. Regarding claim 8, Schmidt/Okamoto discloses the processor of claim 6 wherein the memory interface circuitry is designed to interface with the external memory

Schmidt/Okamoto fails to disclose the use of RAM.

Examiner take Official Notice that random access memory is common, inexpensive and efficient for use in processing systems.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Schmidt/Okamoto and allow a RAM access through the circuitry shown in Okamoto figs. 5, 6, and 7.

10. Regarding claim 9, Schmidt/Okamoto discloses the processor of claim 5 wherein each of the processing units has an input programming element (PE) to read incoming data from any one of the input ports, and output PE to write result data to any one of its output ports, (fig. 3 and col 6 lines 44-55—note that the combination of input and output PEs are considered to be a single programming element) and a core PE to execute instructions independently of data path that is operating through a pair of the input and output ports of that processing unit (fig. 3 pm and st).

11. Regarding claim 11, Schmidt/Okamoto discloses the processor of claim 6 wherein each of the plurality of processing units has a plurality of control ports on each side including an input control port and an output control port (fig. 3 and col 6 lines 44-55), and wherein the input control port of a processing unit is programmable to route incoming command information to any one of the output control ports of the processing unit (col 3 lines 5-7).

12. Regarding claim 12, Schmidt/Okamoto discloses the processor of claim 9 further comprising an interface to an external device (Okamoto figs. 5, 6, and 7), and wherein the output ports of one of said processing units are coupled ot the input ports of an

adjacent one of the processing units except that some of the output ports of an outlying one of said processing units are coupled to the external device interface (fig. 1a with the combination described with respect to claim 1).

13. Regarding claim 13, Schmidt/Okamoto discloses the processor of claim 5 further comprising: a second DMA unit, wherein there are at least four of said plurality of processing units, the data ports on the north side of the first and second ones of said four processing units are coupled to the first DMA unit, the data ports on the south side of third and fourth ones of said four processing units are coupled to the second DMA unit, and the data ports of a south side of the first and second processing units are coupled to the data ports of a north side of the third and fourth processing units.

Note that the first, second, etc DMA units appear to be merely labels and do not significantly limit the claim.

14. Regarding claim 14, Schmidt/Okamoto discloses the processor of claim 13 further comprising an interface to an external device (Okamoto figs. 5, 6 and 7), wherein some of the data ports of east and west sides of the processing units are coupled to the external device (fig. 1a).

Note that the distinction of east and west sides can be altered by physically rotating the apparatus.

15. Regarding claim 15, Schmidt/Okamoto discloses the processor of claim 5 further comprising a control processing unit to read and execute instructions that configure the data ports of the DMA unit to create a data channel from one of the processing units to external memory (fig. 3 with Okamoto figs. 5, 6 and 7).

16. Regarding claim 16, Schmidt/Okamoto discloses the processor of claim 5 further comprising a host interface cunit to receive instructions, from the external host controller, that configure the data ports and the DMA unit to create a data path from one of the processing units to external memory (Okamoto fig. 5 I/O interface).

17. Regarding claim 17, Schmidt/Okamoto discloses a system comprising: a host controller (col 5 lines 35-42), a data driven processor (col 1 lines 13-15) having a memory access unit to interface a external memory (Okamoto figs. 5, 6 and 7), a plurality of processing units each having a plurality of data ports (fig. 1a), the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit (fig. 1a; col 3 lines 5-7), and a host interface unit to receive instructions from the external host controller that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory (fig. 7; col 9 lines 26-49 in combination with Okamoto), wherein one of the processing unit has a control port which it uses to write data location information to the memory access unit (Okamoto col 7 lines 18-28)

Schmidt/Okamoto fails to disclose one of a rechargeable battery and a fuel cell coupled to power the external memory, the host controller, and the data driven processor.

Examiner takes Official Notice that running a device off of a battery allows the device to be used in environments and situations distant from other power sources. Increased mobility is a beneficial feature of the invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have included batteries for power in the system of Schmidt/Okamoto for the benefit of increased mobility/flexibility.

18. Regarding claim 18, Schmidt/Okamoto discloses the system of claim 17 wherein the host controller includes an embedded processor and its associated main memory (Okamoto fig. 5, 6, and 7).

Note that the I/O interface is considered to be a processor.

19. Regarding claim 19, Schmidt/Okamoto discloses the system of claim 17 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection (fig. 1a).

20. Regarding claim 20, Schmidt/Okamoto discloses the system of claim 19 wherein each of the processing units has a core programming element (PE) that can be programmed to execute instructions that operate on incoming data received via an input

data port of that processing unit (fig. 3 pm and st in conjunction with Okamoto figs. 5, 6 and 7), an input PE that can read data from any one of a plurality of input ports of that processing unit, and an output PE that can write data to any one of the plurality of output data ports of the processing unit (fig. 3 and col 6 lines 44-55)

21. Regarding claim 21, Schmidt/Okamoto discloses the system of claim 20 wherein the core PE of each processing unit can execute its instructions independently of a data parth that is operating through a pair of said input and output data ports of the processing unit (fig. 3 col 6 lines 44-55).

22. Regarding claim 22, Schmdit/Okamoto discloses the system of claim 17, but fails to disclose that the data location information that is sent through the control port includes information about the size and display location of a block of image data.

Image location data and size ensure that the image is properly displayed after the processing is completed.

Including image location and size data would have been obvious to one of ordinary skill in the art at the time of the invention for the benefit of ensuring the image appears in the proper location on the display.

23. Regarding claim 23, Schmidt/Okamoto discloses a system comprising an external memory (Okamoto figs. 5, 6 and 7); a data driven processor (col 1 lines 13-15) having a memory access unit to interface the external memory (Okamoto figs. 5, 6 and

7), a plurality of processing units each having a plurality of data ports (fig. 1a), the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units (col 3 lines 5-7) to the memory access unit (Okamoto figs. 5, 6 and 7), and a central processing unit to receive and execute instructions that configure the data ports and memory unit to create a data path from one of the processing units through a data channel to the external memory (col. 2 lines 20-26), wherein one of the processing units has a control port which it uses to write data channel information to the memory access unit (Okamoto figs. 5, 6 and 7); and one of a rechargeable battery and a fuel cell coupled to power the external memory and the data driven processor (see claim 17).

24. Regarding claim 24, Schmidt/Okamoto discloses a system of claim 23 wherein each of the processing units has a plurality of control ports that are connected to each other in a mesh arrangement so that the data channel information, including one of ta read and write command, address, and memory access unit channel identifier, can originate from any one of the processing units and be routed to the memory access unit via a logical control channel programmed in the mesh arrangement (fig. 1a)

25. Regarding claim 25, Schmidt/Okamoto discloses the system of claim 23 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection (fig. 1a).

26. Regarding claim 26, Schmidt discloses the system of claim 23 wherein each of the processing units has a plurality of control ports that are coupled to each other and are programmable to allow data channel information to be sent from any one of the processing units to the memory access unit (Okamoto figs. 5, 6 and 7).

27. Regarding claim 27, Schmidt/Okamoto discloses a data processor comprising: means for translating higher level read and write commands into lower level memory access commands (fig. 8a—*note that the memory instructions of Schmidt/Okamoto require the use of switching data streams, which is considered to be a lower level memory access command*); a plurality of means for consuming data (col 9 lines 26-49); means for implementing programmable data paths to supply data to and accept data from any one of the plurality of data consumption means (col. 3 lines 5-7); means for receiving instructions (col 9 lines 26-49), from other than said plurality of data consumption means (Okamoto figs. 5, 6 and 7), to configure the programmable data path implementation means, the plurality of data consumption means, and the higher level read and write translation means; and means for implementing a programmable control path through said plurality of data consumption means to transfer higher level read and write commands from one of said plurality of data consumption means to the higher level read and write translation means (fig. 8a—*again, considered to be the switch control signals*).

28. Regarding claim 28, Schmidt/Okamoto discloses the processor of claim 27 further comprising means for ensuring that said lower level memory accesses meet signal level and timing requirements of external memory.

Note that is inherent that the signal level and timing requirements are met in order to ensure proper communication between the processing unit and the external memory.

29. Regarding claim 29, Schmidt/Okamoto discloses the processor of claim 27 further comprising means for expanding the data processor (col 3 lines 51-55).

Response to Arguments

30. Applicant notes that rejection of the independent claim was not entirely clear. Examiner will attempt to clarify the issue.

31. Claim 1 discloses "A data driven processing method, comprising: providing a first set of instructions and incoming data to the first processing unit, of a data driven processor, to operate upon said incoming data."

Examiner has pointed to Fig. 7 and col 9 lines 26-49. Both indicate a description of the instruction being sent to each processing unit shown in figures 1 and 2. The "data driven" portion is also explicitly disclosed in col 1 lines 13-15.

Claim 1 further discloses, "to operate upon said incoming data; configuring a data path for transferring data between a second processing unit of the data driven processors.

Examiner's citation of col 4 lines 37-40 shows that information from one processing unit is sent to other processing units. Before the combination, this is done directly from a local FIFO memory (col 2 lines 12-20; Fig. 2 FIFO MEMORY). This will be changed to some degree after the combination.

Claim 1 further discloses, "and the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to memory, provides addressing information to a memory access unit of the processor"

Here, it is clear that memory instructions -- like loads and stores -- exist (col 2 lines 20-26; col 1 lines 64-66). Indeed, they exist in most every processor. And after the combination of external memory, the address bits shown in col 9 lines 26-49 will be used to address the external memory found in Okamoto (figs. 5, 6 and 7).

Claim 1 further discloses, "to enable the transfer of additional data between the external memory and the second processing unit via said data path."

This is perhaps where the confusion arose. "Said data path" initially referred to the connection between the processing units shown, for example, in Fig. 8a reference 48. This has been altered to some degree by the combination. Now, "said data path" refers to the connection from the second processing unit to the external memory added by Okamoto. The "additional data" refers to the value that was stored into the memory by the memory (or even arithmetic) operations by the first processing unit. This data is

later taken by the second processing unit in a way analogous to the original design using only local FIFO memory (col 4 lines 37-40).

32. Applicant further states:

> *"As far as Applicants are aware, in a conventional data driven processor, a built-in host controller assists the processor by orchestrating the feeding of instructions and incoming data to individual processing elements (processing units) of the data processor. It is also this host controller that identifies sequentially addressed locations in external memory to which, for instance, an outgoing stream of data from the data processor is written. In that situation, a processing element or cell (processing unit) of the data driven processor is not aware of the particular address or source of the incoming data, nor does it know where, that is what address or location in external memory, its result data is ultimately destined. Okamoto is silent on this issue and therefore lacks the teaching needed to render claim I obvious."*

This does not appear to be how Schmidt is designed. The instructions are provided locally in a program memory (Fig. 2 PROGRAM MEMORY; col 9 lines 26-27). Moreover, the destination address is located in fields 6-10 of the instruction bits (Fig 7; col 9 lines 50-52). Therefore, it seems logical that with the addition of an external memory, these destination bits would be send from the first processing unit to the memory access unit.

33. With respect to claim 5, Applicant argues about the existence of a DMA unit in Schmidt. Direct memory access is a feature of modern processors that allows certain hardware subsystems within the computer to access system memory independently of the central processing unit. Indeed, Fig. 3 does not appears to use DMA for memory access. This functionality carries over to the combination with Okamoto while including the external memory.

34. With respect to claims 17 and 23, Applicant argues "a control port which it uses to write data channel information to the memory access unit" and "a control port which it uses to write data location information to the memory access unit". The terms "data channel information" and "data location information" are somewhat unclear, but appear to be referring to addressing information, which is located in the address bits of the instruction in the local program memory and must be sent to the external memory (including its memory access unit) in order to properly read and write instructions.

35. With respect to claim 27, Applicant argues the limitation, "means for implementing a programmable control path through the plurality of data consumption means to transfer higher level read and write commands from one of the data consumption means to the higher level read and write translation means." Examiner notes that this limitation is somewhat confusion. For example, the term "data consumption" is never used in Applicant's Specification beyond the claims.

Regarding the interpretation, a "higher level" read and write command is the general command required to send a piece of data to a particular address. This is translated into lower level switch signals – the switch signals used to run the multiplexers, a component necessary for the processor to determine where to store the data based on the original address information – by means of some sort of combinational logic. This combinational logic is the "higher level read and write translation means".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183